

Evaluation of Lead-free Solders, Halogen-free Laminates, and Nanomaterial Surface Finishes for Assembly of Printed Circuit Boards for High Reliability Applications

Gregory Morose¹, Sammy Shina², Robert Farrell³, Michael Ellenbecker², and Rafael Moure-Eraso²

¹Massachusetts Toxics Use Reduction Institute, Lowell, Massachusetts, ²University of Massachusetts Lowell, Lowell, Massachusetts, ³Benchmark Electronics, Hudson, New Hampshire

Key Words: Lead-Free, Halogen-Free, Nanomaterials, Printed Circuit Boards, RoHS, DoE

Abstract

For the past several years, there has been a global effort in the electronics industry to move towards using lead-free materials for the production of printed circuit boards (PCB's). However, there are numerous technical and economic challenges that remain to hinder the universal implementation of lead-free materials, especially for high reliability electronics applications

The research presented in this paper was conducted by the members of the New England Lead-free Electronics Consortium. The objective of this research was to evaluate the solder joints of electronics assemblies produced with various lead-free and halogen-free materials for use in high reliability applications. Visual inspection procedures for this research meet IPC Class 3 standards for High Performance Electronics Products. This Class 3 standard is used for inspecting electronics assemblies used for high reliability applications. The lead-free materials that were evaluated during the assembly included four PCB surface finishes (ENIG, OSP, HASL, and nano), two through hole technology (THT) solders (tin/silver/copper, and tin/copper), and three different surface mount technology (SMT) solder pastes based on the SAC305 alloy. In addition, a halogen-free laminate material was also evaluated. The results of the lead-free assemblies were compared against baseline data obtained by assembling test vehicles with tin/lead materials.

In summary, the assembly of lead-free electronics for high reliability applications is achievable with equal or less solder joint defects than tin/lead assemblies. This is possible with the careful selection of both lead-free solder and surface finish materials.

Introduction

The major types of drivers for moving manufacturers towards lead-free electronics include regulatory and market drivers. The major regulatory driver has been the European Union's Restriction on the use of certain Hazardous Substances (RoHS) Directive that was enacted in 2003. This directive limits the amount of lead and five other substances that are used in electrical and electronic equipment. These amounts are

listed in Table 1 below. The RoHS directive covers some, but not all, electrical and electronic equipment placed on the European Union market as of July 2006. There are several types of electronics products that are either exempt or considered out of scope from this directive. This includes electronics products requiring high reliability such as network infrastructure, aerospace, defense, and medical applications [1]. These high reliability applications are the focus of this research. Because of these exemptions, there is continued use of lead in the electronics industry for many products sold in the European Union. [2]

Substance	Maximum Concentration
Lead	< 1,000 ppm
Mercury	< 1,000 ppm
Cadmium	< 100 ppm
Hexavalent Chromium	< 1,000 ppm
Polybrominated biphenyls	< 1,000 ppm
Polybrominated diphenyl ethers	< 1,000 ppm

Table 1: RoHS Directive Maximum Concentrations

The objective of this research was to evaluate the solder joints of electronics assemblies produced with various lead-free and halogen-free materials for use in high reliability applications. The defect level of the lead-free assemblies was compared to the tin/lead assemblies. Visual inspection procedures for this research meet IPC Class 3 standards for High Performance Electronics Products. This Class 3 standard is used for inspecting electronics assemblies used for high reliability applications. For lead-free electronics, it is desirable to be able to assemble PCBs with lead-free solder joints that have equal or less defects than PCBs assembled with tin/lead solder. Subsequent research by the Consortium will be conducted in the future to further evaluate the long-term reliability of these test vehicles by using accelerated testing techniques.

Experimental Procedure

The assembly of 35 test vehicles occurred during 2008 at the Benchmark Electronics facilities in Hudson, New Hampshire and Guadalajara, Mexico. The test vehicle shown in Figure 1 is eight inches wide by ten inches long, contains 20 layers, is 0.110 inches thick, and is densely populated on both sides with SMT and THT components. The test vehicle included a number of thermally disparate Surface Mount Technology (SMT) components which made assembly challenging. The results are applicable for similar sized PCBs

and can be extrapolated to thinner, less thermally disparate PCBs which are more common in the electronics industry.

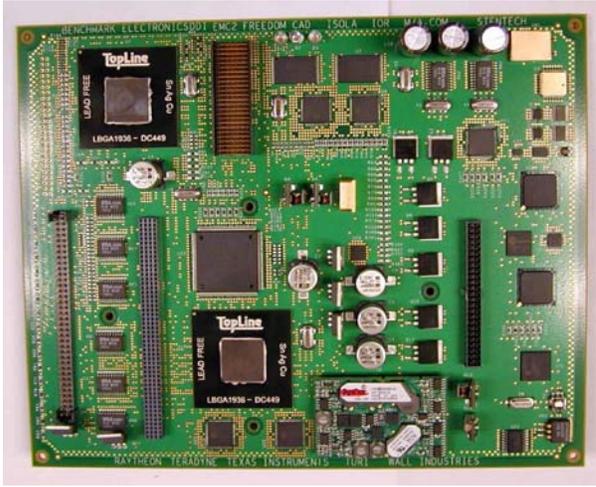


Figure 1: Assembled Test Vehicle

There were 886 SMT components (BGAs, microBGAs, resistors, TSOPs, PQFPs, PQFN, and MLFs), and 21 THT components (connectors, LEDs, DC/DC converters, and capacitors) assembled on each test vehicle. Table 2 provides the component counts for the total amount of SMT and THT components used for the assembly of the test vehicles.

Table 2: Component Counts for Test Vehicle Assembly

Component Type	Components Per Board	Lead-free DOE (24 test vehicles)	Tin/Lead DOE (8 test vehicles)	Halogen-free (3 test vehicles)
Surface mount	886	21,264	7,088	2,658
Through hole	21	504	168	63
Totals	907	21,768	7,256	2,721

This research included four different PCB surface finishes.

1. Electroless Nickel Immersion Gold (ENIG). This surface finish involves using both electroless and immersion technologies to deposit the metallic surface finish.
2. Hot Air Solder Leveling (HASL). For this research, the surface finish used the lead-free alloy Sn100C that is comprised of mostly tin, but also includes 0.6% copper, 0.05% nickel, and 0.0055% germanium.
3. Organic Solderability Preservatives (OSP).
4. Nano materials surface finish using nanosilver particles dispersed in a polymer (polyaniline), with a thickness between 45 to 65 nm. This was selected because it has the potential of addressing major lead free implementation challenges such as copper dissolution during rework and process improvement for assembly of lead-free THT components. Moreover, this finish uses significantly less silver as compared with a standard (non-nanotechnology based) silver finishes and is

applied at lower temperatures which makes it environmentally more friendly and less thermally stressful to the PCB.

This research included the following three different solder pastes for assembly of the SMT components.

1. Tin/silver/copper alloy (SAC305) with no clean chemistry flux (from two different suppliers)
2. Tin/silver/copper alloy (SAC305) with organic acid chemistry flux
3. Tin/lead alloy with no clean chemistry flux for baseline purposes

Three different solder alloys were used in this research for the assembly of the THT components. The solders to be used are as follows:

1. Tin/silver/copper alloy (SAC305)
2. Tin/copper alloy (Sn100C) using two different assembly operation settings. This solder has the same composition as the HASL alloy.
3. Tin/lead alloy for baseline purposes

Two different laminate materials were used for this research:

1. The first FR-4 laminate material was designed for use in lead-free assembly environments and has a glass transition (T_g) temperature of 180 degrees C. This laminate material was used for the 32 test vehicles included in the Design of Experiments.
2. Three test vehicles were assembled using laminate material with halogen-free flame retardants and a glass transition (T_g) temperature of 180 °C.

Design of Experiments (DoE) is a systematic method for determining the effect of factors and their possible interactions on a design or process. [3] A factor is a variable that is studied at different levels in a designed experiment. Levels are the different amounts or types included in each factor used in a designed experiment. For this research, the three factors under investigation in the DoE were SMT solder paste, THT component solder, and surface finish. The four levels for the through THT solder factor were the SAC 305 tin/silver/copper alloy, Sn100C tin/copper alloy (at two different operational settings), and tin/lead alloy. The four levels for the SMT component solder paste were tin/silver/copper alloy (SAC305) with no clean flux (two different manufacturers used), tin/silver/copper alloy (SAC305) with organic acid flux, and tin/lead alloy with no clean flux. The four levels for the surface finish were ENIG, OSP, nano, and lead-free HASL. Table 3 shows the total of 24 lead-free experiments used in this research.

Table 3: Lead-free Test Vehicles - Design of Experiments

Test Vehicle	SMT Solder Paste	Through Hole Solder	Surface Finish	PWB Laminate
1	SAC305 No Clean (1)	SAC305	ENIG	High Tg FR4
2	SAC305 No Clean (1)	SAC305	ENIG	High Tg FR4

Test Vehicle	SMT Solder Paste	Through Hole Solder	Surface Finish	PWB Laminate
3	SAC305 No Clean (1)	SAC305	LF HASL	High Tg FR4
4	SAC305 No Clean (1)	SAC305	LF HASL	High Tg FR4
5	SAC305 No Clean (1)	SAC305	OSP	High Tg FR4
6	SAC305 No Clean (1)	SAC305	OSP	High Tg FR4
7	SAC305 No Clean (1)	SAC305	Nano-finish	High Tg FR4
8	SAC305 No Clean (1)	SAC305	Nano-finish	High Tg FR4
9	SAC305 Org. Acid	Sn100C (295 C)	ENIG	High Tg FR4
10	SAC305 Org. Acid	Sn100C (295 C)	ENIG	High Tg FR4
11	SAC305 Org. Acid	Sn100C (295 C)	LF HASL	High Tg FR4
12	SAC305 Org. Acid	Sn100C (295 C)	LF HASL	High Tg FR4
13	SAC305 Org. Acid	Sn100C (295 C)	OSP	High Tg FR4
14	SAC305 Org. Acid	Sn100C (295 C)	OSP	High Tg FR4
15	SAC305 Org. Acid	Sn100C (295 C)	Nano-finish	High Tg FR4
16	SAC305 Org. Acid	Sn100C (295 C)	Nano-finish	High Tg FR4
17	SAC305 No Clean (2)	Sn100C (310 C)	ENIG	High Tg FR4
18	SAC305 No Clean (2)	Sn100C (310 C)	ENIG	High Tg FR4
19	SAC305 No Clean (2)	Sn100C (310 C)	LF HASL	High Tg FR4
20	SAC305 No Clean (2)	Sn100C (310 C)	LF HASL	High Tg FR4
21	SAC305 No Clean (2)	Sn100C (310 C)	OSP	High Tg FR4
22	SAC305 No Clean (2)	Sn100C (310 C)	OSP	High Tg FR4
23	SAC305 No Clean (2)	Sn100C (310 C)	Nano-finish	High Tg FR4
24	SAC305 No Clean (2)	Sn100C (310 C)	Nano-finish	High Tg FR4

The DoE (including solder paste, solder, surface finish, and laminate material) that was used for the eight tin/lead test vehicles is provided in Table 4. These tin/lead test vehicles provided a baseline for comparison with the lead-free test vehicles.

Table 4: Tin/lead Boards - Design of Experiments

Test Vehicle	SMT Solder Paste	Through Hole Solder	Surface Finish	PWB Laminate
25	Tin Lead No Clean	Tin/Lead	ENIG	High Tg FR4
26	Tin Lead No Clean	Tin/Lead	ENIG	High Tg FR4
27	Tin Lead No Clean	Tin/Lead	LF HASL	High Tg FR4
28	Tin Lead No Clean	Tin/Lead	LF HASL	High Tg FR4
29	Tin Lead No Clean	Tin/Lead	OSP	High Tg FR4
30	Tin Lead No Clean	Tin/Lead	OSP	High Tg FR4
31	Tin Lead No Clean	Tin/Lead	Nano- finish	High Tg FR4
32	Tin Lead No Clean	Tin/Lead	Nano- finish	High Tg FR4

In addition, three halogen-free test vehicles were assembled, but were not included within the DoE. The solder paste, solder, surface finish, and laminate materials that were used for the three halogen-free test vehicles are provided in Table 5.

Table 5: Halogen-free Boards

SMT Solder Paste	Through Hole Solder	Surface Finish	PWB Laminate
SAC305 No Clean (1)	SAC305	OSP	Halogen free FR4
SAC305 No Clean (1)	SAC305	OSP	Halogen free FR4
SAC305 Org. Acid	SAC305	OSP	Halogen free FR4

Printing and Placement Process

The equipment used for printing operations was the DEK 265 printer using Instintiv software. The bottom stencil used for this research was an electroformed nickel stencil with a thickness of 0.005”, and the top stencil was an electroformed nickel stencil with a thickness of 0.004”. The printing parameters used on the DEK 365 printer included a print speed of 0.51 inches per second, a front and rear blade pressure of 19.404 pounds, a separation speed of 0.055 inches per second, and a separation distance of 0.098 inches. These printing parameters were used for assembly of all the lead-free and tin/lead test vehicles. The GSM Genesis machine was used for placing the SMT components.

Reflow Process

The equipment used for reflow operations was the Vitronics Soltec XPM2 reflow oven with ten heating zones and three cooling zones, using Vitronics X2series XN1030

software. All profiles were done in an air environment which is less expensive and more prevalent in the industry than a nitrogen atmosphere. The thermal profile used for the tin/lead and lead-free test vehicles was a ramp to peak profile. Six thermocouples were attached to various locations of a spare test vehicle to develop the desired thermal profiles. Table 6 provides the component and test vehicle location information for the six thermocouple locations for the bottom side of the test vehicle.

Table 6: Test Vehicle Bottom Side Thermocouple Locations

Thermocouple	Component Type	Reference Designator	Location on Test Vehicle
1	Resistor	RN12	Leading edge, center
2	Capacitor	C9	Center, right side
3	Resistor	RN9	Trailing edge, left side
4	Thin small outline package (TSOP)	U24	Center, left side
5	TO220	Q22	Trailing edge, center
6	Not applicable	Laminate	Center

There were six thermocouple locations used for developing the thermal profile for reflow of the top side of the test vehicle. Table 7 provides the component and board location information for these six thermocouple locations.

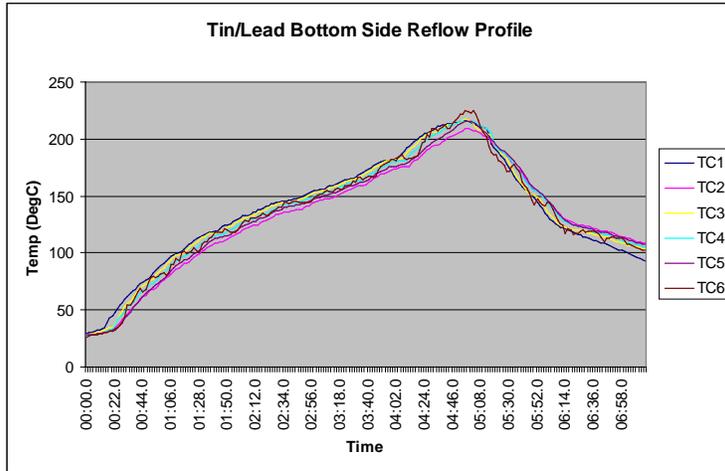
Table 7: Test Vehicle Top Side Thermocouple Locations

Thermocouple	Component Type	Reference Designator	Location on Test Vehicle
1	Thin shrink small outline package (TSSOP)	U5	Trailing edge, right side
2	Capacitor	C3	Center
3	Resistor	RN5	Leading edge, center
4	Small outline	U23	Trailing edge, left side
5	Thin small outline package (TSOP)	U1	Trailing edge, center
6	Ball grid array (BGA)	U19	Center, left side

The first temperature profile was developed for tin/lead test vehicles. The melting temperature for tin/lead solder is 183 °C. The target peak temperature in the reflow oven for test vehicles assembled with tin/lead solder is in the range of 210 to 218 °C, and the

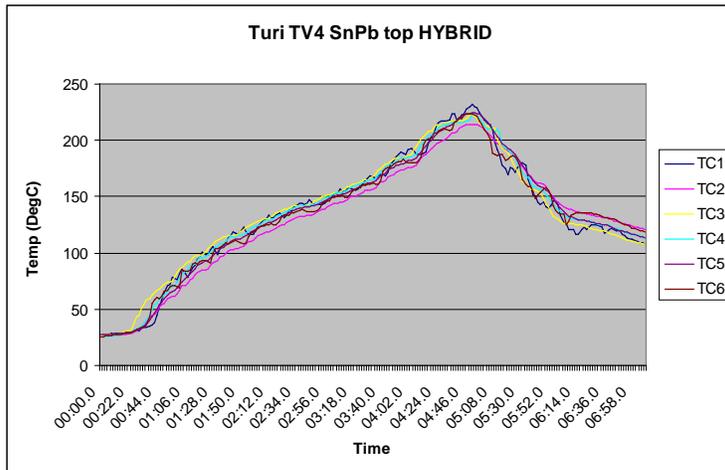
target time above liquidus (TAL) temperature is in the range of 60 to 90 seconds. The actual bottom side temperature profile for each of the six thermocouple locations can be seen in Figure 2.

Figure 2: Bottom Side Reflow Profile for Tin/Lead Boards



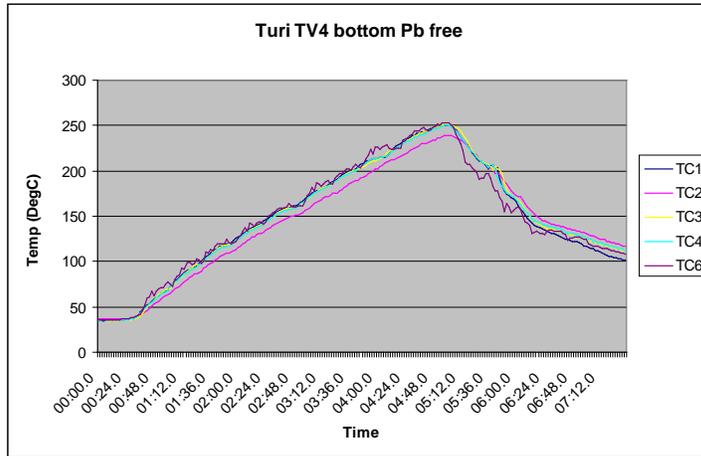
The second temperature profile generated was for the top side of the test vehicles assembled with tin/lead solder paste. The top side of the test vehicles contains BGA components that have lead-free solder balls. Therefore, a hybrid temperature profile was needed to melt the tin/lead solder pastes as well as the lead-free solder on the BGA components. The target peak temperature for the hybrid profile was in the range of 222 to 230 °C, and the target TAL was in the range of 60 to 90 seconds [4]. The actual top side temperature profile for each of the six thermocouple locations can be seen in Figure 3.

Figure 3: Top Side Reflow Profile for Tin/Lead Boards



The third temperature profile generated was for the lead-free test vehicles. Lead-free solder paste using the SAC 305 tin/silver/copper alloy solder melts between 217 and 221 °C. All three lead-free solder pastes in this research contained the SAC 305 alloy. The target peak temperature for boards assembled with lead-free solder is in the range of 240 to 248 °C, and the target TAL is in the range of 60 to 90 seconds [5]. The actual bottom side lead-free temperature profile for each of the six thermocouple locations can be seen in Figure 4.

Figure 4: Bottom Side Reflow Profile for Lead-free Boards



Assembly of Through Hole Components

The equipment used for this step was the Vitronics My Selective 6748 and 6749 soldering machines. This equipment has robotic multiwave and selectwave soldering capability and both methods were used for creating the solder joints for all the through hole components on the test vehicles.

The selectwave process uses a robot system to pick up, hold, and drag the test vehicle over a single nozzle wave. The single nozzle is stationary and the size of the single nozzle can be varied depending upon the requirements of a particular application. The robot system is capable of moving and tilting the test vehicle across the nozzle with high precision and consistency. The selectwave process has the advantage of being able to solder in tight locations, and it can also provide different drag speeds for each of the through hole components. A disadvantage is the long time needed to solder multiple parts. This extended time can result in solderability issues due to the cooling of the printed circuit board during this time. The selectwave process is sometimes referred to as “single point” or “single wave”.

The multiwave process uses a robot system to pick up, hold, and dip the test vehicle onto multiple nozzles that are mounted on a product specific nozzle plate. The test vehicles were held over the nozzles for a predetermined time, referred to as “dwell time”. The multiwave process has the advantage of soldering multiple THT components at the same time. However, the dwell time cannot be varied for individual components that may require more or less time over the nozzle to achieve a quality solder joint. The preheating of the test vehicle is necessary to minimize the thermal stress that occurs when the test vehicle is exposed to the high soldering temperatures. The intent is to

gradually raise the temperature of the test vehicle closer to the soldering temperature to minimize thermal stress. However, the preheat temperature cannot be too high or it may burn off the flux before the soldering occurs. Therefore, the target preheat temperature used for this research was between 110 to 115° C. A summary of the soldering parameters used for the thirty-two lead-free and tin/lead test vehicles in the DoE are provided in Table 8.

Table 8: Through Hole Soldering Parameters

Parameter	SAC 305	Sn100C (1)	Sn100C (2)	Tin/Lead
Test Vehicle Number	1 - 8	9 - 16	17 - 24	25 - 32
Flux	Alpha 3215 NC	Alpha 3215 NC	Alpha 3215 NC	Hi Grade 1076-30 NC
Preheat	110 – 115 °C			
Multiwave Pot Temp.	295 °C	295 °C	310 °C	270 °C
Multiwave Dwell Time	13 seconds	13 seconds	16 seconds	7 seconds
Selectwave Pot Temp.	300 °C	300 °C	310 °C	270 °C
Selectwave Nozzle Size	8 mm	8 mm	8 mm	4 mm

The drag speeds used during the selectwave process were varied for the different component types and the different solder alloys. Table 9 provides the drag speeds used for the various component types and solders.

Table 9: Selectwave Drag Speeds

Components	SAC305 (mm/sec)	Sn100C (1) (mm/sec)	Sn100C (2) (mm/sec)	Tin/Lead (mm/sec)
Test Vehicle Number	1 - 8	9 - 16	17 - 24	25 - 32
Capacitors	1.2	1.2	1.0	1.0
LEDs	1.2	1.2	1.0	1.0
TO220	2.0	2.0	1.7	5.0
DC/DC Converter	0.7	0.7	0.5	0.5

Inspection

The inspection effort included both visual and automated X-ray inspection. The IPC-A-610 Revision D standard was used as the guideline for conducting the visual inspection for this research. A defect is defined by this standard as a condition that may be insufficient to ensure the form, fit or function of the assembly in its end use environment.

The visual inspection was conducted to meet the requirements of Class 3: High Performance Electronic Products. This classification was chosen because it covers electronics assemblies that must meet high reliability applications. The definition of Class 3: High Performance Electronic Products is as follows: “includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support and other critical systems [6].

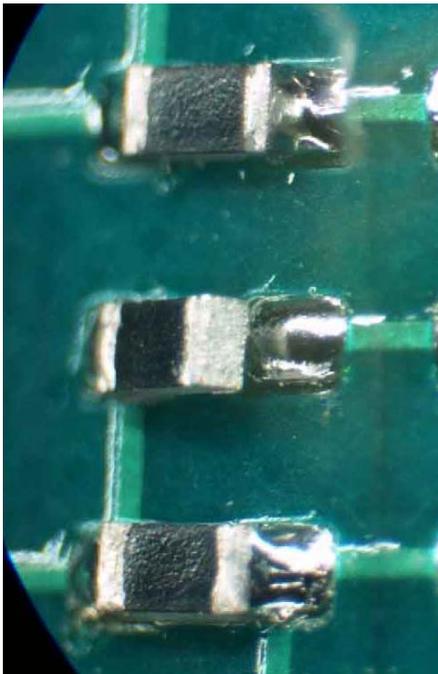
The visual inspection included the solder joints, the laminate, and components with the latter two being inspected for thermal degradation which is necessary because lead free processing temperatures are approximately 30 °C higher as compared to assembly with tin/lead solder. The HP/Agilent 5DX X-ray system was used for the automated X-ray inspection. All assembly defects identified during the inspection process were at the component lead level. For example, if defects were found on three different leads of a single component, then the total defect count would be three.

Results and Discussion

SMT Component Analysis:

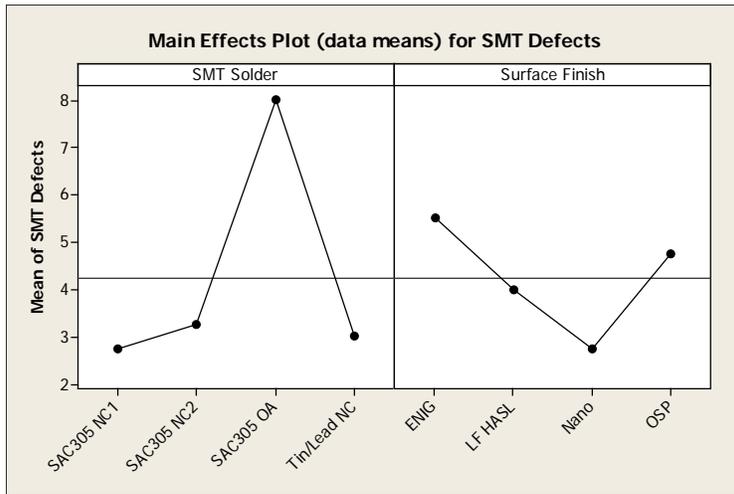
A total of 145 SMT component defects were identified on the thirty-five test vehicles resulting in an overall mean defect rate of 4.1 defects per test vehicle. The printed circuit boards, components, and flux residues (no-clean only) did not exhibit any signs of thermal degradation. Figure 5 shows an example of a surface mount component defect identified during this research. The resistor located at R1 on test vehicle is shown with a tombstone defect. R1 is the middle resistor in the picture.

Figure 5: Tombstone Defect on Test Vehicle 29



Minitab Software was used to generate all the statistical data and plots for this research. Upon review of the main effects plot for SMT components shown in Figure 6, it can be seen that the SAC 305 OA solder paste had a much higher mean defect rate (8.0 defects per board) than the overall average of 4.1 defects per board. The other three solder pastes had defect rates between 2.7 and 3.2 defects per board. For the surface finishes, it can be seen that the nano surface finish had the lowest mean defect rate (2.7 defects per board), while the other three surface finishes had defect rates between 4.0 and 5.5 defects per board.

Figure 6: Main Effects Plot for SMT Components



Another important consideration to investigate is the effect of interaction between factors that may have an impact on the results. The interaction results for SMT components are shown in Figure 7. The combination with the lowest mean defect level was the tin/lead solder paste and the nano surface finish with zero defects per test vehicle. The combination with the highest defect level was the SAC 305 OA solder paste and the OSP finish with 10 defects per test vehicle.

This interaction plot is interesting because it shows that although the nano surface finish had the lowest overall defect rate, it had the highest defect rate for the SAC 305 NC2 solder paste. This plot also reveals that the Lead-free HASL surface finish had the lowest defect rate for both the SAC 305 NC1 and SAC 305 NC2 solder pastes. Based upon the results of this plot it can be stated that the Lead-free HASL was the best performing finish for lead-free no clean solder pastes, and that the nano finish was the best performing finish for the lead-free OA and tin/lead solder pastes.

Figure 7: Interaction Plot for Surface Mount Component Defects (All Solders)

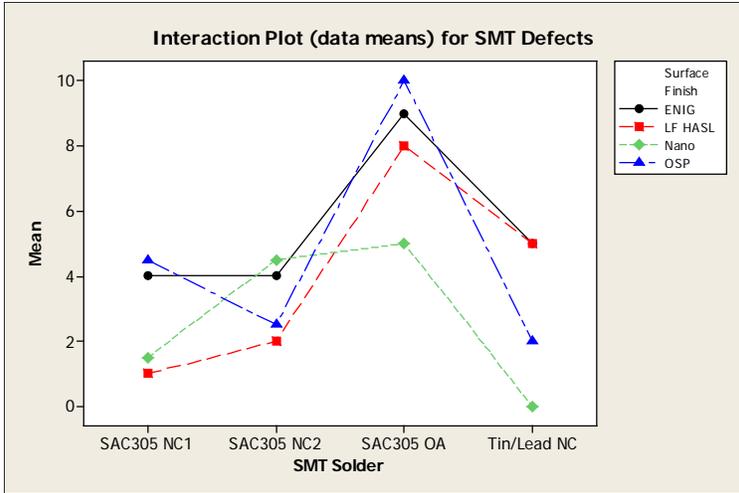


Figure 8 is a Pareto Chart for the SMT component defect types for lead-free test vehicles only. This chart reveals that solder bridges, unsoldered leads, insufficient solder, and non-wetting to component were the most prevalent defect categories. The “Other Category” includes two voiding defects, one solder splatter defect, one non-wetting to pad defect, and one tombstoned defect.

Figure 8: Pareto Chart for SMT Component Defect Types for Lead-free Test Vehicles

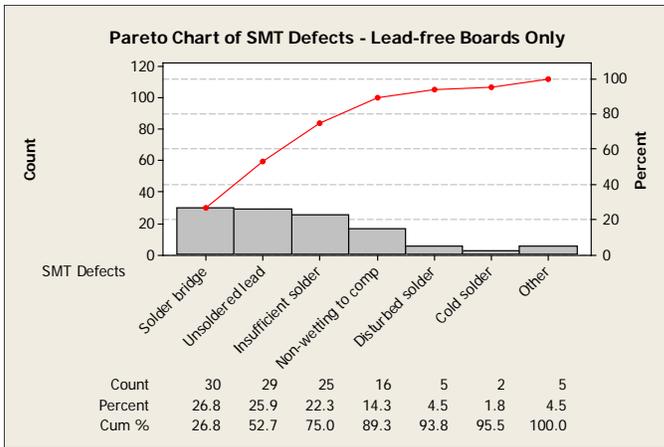


Table 10 shows the relationship between the SMT component defect types for lead-free test vehicles and the four different surface finishes. For example, for the insufficient solder defect, the best performing surface finish was lead-free HASL with only one defect. For this defect type, the OSP surface finish had the highest number of defects with sixteen defects.

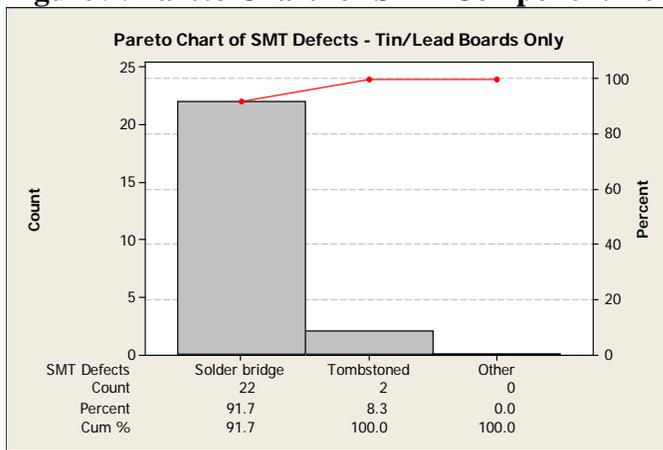
Table 10: Component Defect Types by Surface Finish

Surface Finish	Solder Bridge	Unsoldered Lead	Insufficient Solder	Non-wetting to Component
ENIG	30	29	25	16
LF HASL	1	1	1	1
Nano	1	1	1	1
OSP	1	1	1	1

Surface Finish	Solder Bridge	Unsoldered Lead	Insufficient Solder	Non-wetting to Component
ENIG	11	11	5	3
LF HASL	7	5	1	6
OSP	7	4	16	7
Nano	5	9	3	0
Total	30	29	25	16

Figure 9 is a Pareto Chart for the surface mount component defect types for tin/lead test vehicles only. The chart reveals that solder bridges and tombstoning were the only defect categories found for tin/lead test vehicles.

Figure 9: Pareto Chart for SMT Component Defect Types for Tin/lead Test Vehicles

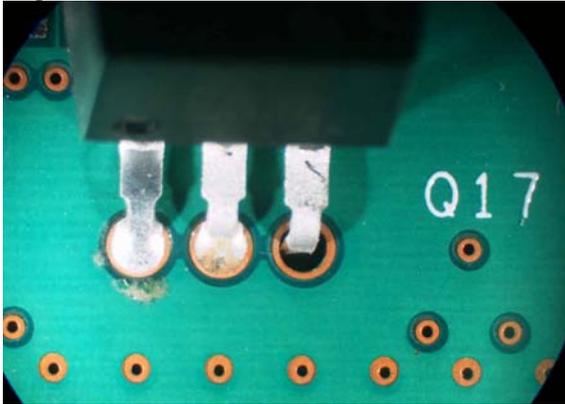


The three halogen-free test vehicles that were assembled had only one surface finish (OSP) and two different solder paste materials (SAC305 NC1 and SAC305 OA). Consequently, only four test vehicles (numbers 5, 6, 13, and 14) in the Design of Experiments with an OSP finish and either the SAC 305 NC1 or SAC305 OA solder pastes were used for the comparison with the halogen free boards. The mean defect level for the four selected High T_g FR4 laminate material (7.2 defects per board), was more than twice as high as the mean defect level for the halogen free laminate material (3.0 defects per board).

THT Component Analysis

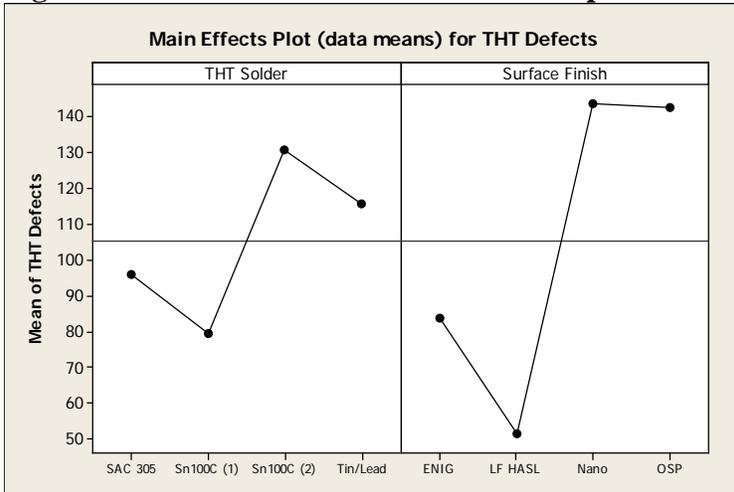
Due to drift that occurred during the multiwave operations, only sixteen test vehicles were included in the THT DOE (only one replicate for each combination). A total of 1,685 THT component defects at the lead level were identified, and the overall mean for defects per board for all DoE combinations was 105.3 defects per test vehicle. Figure 10 shows an example of a THT component defect identified during this research and illustrates the insufficient solder defect for one of the leads of component Q17 on the topside of test vehicle number 22.

Figure 10: Insufficient Solder on Test Vehicle Number 22



The two best performing solders were Sn100C (1) and the SAC305 solders with 79.25 and 95.75 defects per test vehicle respectively. The two lesser performing solders were tin/lead and Sn100C (1) solders with 115.5 and 130.7 defects per test vehicle respectively. The two best performing surface finishes were lead-free HASL and ENIG surface finishes with 51.5 and 83.7 defects per test vehicle respectively. The two lesser performing surface finishes were the OSP and nano surface finishes with 142.5 and 143.5 defects per test vehicle respectively. The results of the main effects are shown in Figure 11.

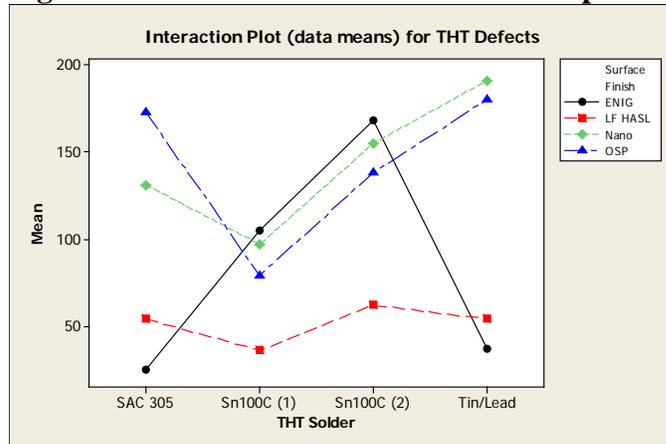
Figure 11: Main Effects Plot for THT Component Defects



The interaction plot for the THT DoE reveals that the ENIG surface finish had the lowest defect rate when using the SAC305 and tin/lead solders. However, the ENIG surface finish had the highest defect rate when used with the Sn100C (1) and Sn100C (2) solders. The lead-free HASL had the lowest defect rate for the Sn100C (1) and Sn100C (2) solders. This positive result was expected given that the lead-free HASL finish is comprised of the Sn100 solder alloy. The performance of the nano and OSP surface

finishes were comparable for each of the four solders. Figure 12 illustrates the effect of the THT DoE interactions for the various combinations.

Figure 12: Interactions Plot for THT Component Defects



The next step in analyzing the results of the THT component assembly was to determine the type of defects that occurred. For the tin/lead boards, 98.5% of the defects were either insufficient solder or solder bridging. For the assembly of THT components with lead-free solder, the most prevalent defect type was insufficient solder (53.6%), the second most prevalent was solder bridge (37%), and the third most was solder splatter (5.5%).

In addition, a comparison was made of the THT components in the three halogen-free test vehicles versus the corresponding two test vehicles (numbers 5 and 6) in the DoE that had similar factors. The mean defect level for the High T_g FR4 laminate material (177.5 defects per test vehicle), was 36% more than the mean defect level for the halogen free laminate material (130.3 defects per test vehicle).

Conclusions

SMT Solder Paste Conclusions:

- For assembly of test vehicles using SMT components, no statistically significant difference was found for the 3 solders or within the 4 surface finishes used.
- Overall, the test vehicles assembled with the SAC 305 NC1 solder paste had the lowest defect rate for all the solder pastes evaluated in this research.
- For test vehicles assembled with lead-free solder pastes, the nano and lead-free HASL surface finishes had the lowest defect rate.
- For the various lead-free solder paste and surface finish combinations, the combination of SAC305 NC1 solder paste and the lead-free HASL surface finish had the overall lowest defect rate for the test vehicles assembled for this research.

THT Solder Conclusions:

- For the assembly of test vehicles using THT components, there was no statistically significant difference for the type of solder, but there was a statistically significant difference for the type of surface finish.
- The most prevalent defect categories identified for THT components were solder bridging and insufficient solder.
- Overall, the test vehicles assembled with the Sn100C-1 (first operating parameters) solder had the lowest defect rate for all three solders evaluated in this research.
- For test vehicles assembled with lead-free solders, Sn100C-1 solder had the lowest defect rate, and the HASL surface finish had the lowest defect rate.
- There was significant variation with the performance of the ENIG surface finish with the various solders. For the tin/lead and SAC305 solders, ENIG was the surface finish with the least defects, and for both Sn100C solder parameters, ENIG was the surface finish with the most defects.

Surface Finishes Conclusions:

- For THT component assembly, the test vehicles assembled with the OSP and nano surface finishes had the highest level of defects. For the test vehicles with an OSP finish, a contributor to this high failure rate was the time delay between conducting the SMT component assembly and THT component assembly. During this delay, there is potential for degradation of the OSP surface finish that can have a negative impact on subsequent soldering efforts. A key recommendation is to try to minimize the time delay between SMT and THT component assembly efforts. Preferably, both efforts should be conducted during the same day.
- The best method for applying the nano surface finish to PCBs is to apply it directly to bare copper. However, for the test vehicles used in this research, this method was not followed. Instead, an OSP finish was first applied to the test vehicle, then the OSP finish was stripped off, and then the nano surface finish was applied to the test vehicles. The soldering results would most likely be better if the nano surface finish is applied directly to bare copper for further research or assembly efforts.

Overall Conclusions

- The defect rate was much higher for THT components than for SMT components. This indicates that further process optimization is needed for assembly of THT components using lead-free materials.
- The IPC Class 3 standard for high reliability applications was used for inspecting the test vehicles assembled for this research. The assembly of lead-free electronics for high reliability applications is achievable with equal or less solder joint defects than tin/lead assemblies. This is possible with the careful selection of both lead-free solder and surface finish materials.

Acknowledgements

The authors would like to acknowledge the contributions from the following individuals and corporations for their support of this research:

Les Garrett, Sharon Xu, Luciana Neves, Mark Karczewski, Robert Lord, Gil Gilcreast, Lisa Wentzell, Vernon Francis, Nina Kasatsky, John Goulet, JoAnn Newell, Paul Bodmer, Eduart Pengu, Bruce Tostevin, Ryan Teeboom, Bryon Macsweeney, Gregory Cronkhite, Nathan Taylor, George Blais Jr., Sidney Collings, Allen Ouellette, Maz Adl-Zarabi, Bea Sybert, Scott Mazur, Debra Ambrosino, and Dorothy Durivage, Benchmark Electronics, Hudson, NH; Edgar Munoz, and Francisco Roman Abreu, Benchmark Electronics Guadalajara, Mexico; Mike Havener, Benchmark Electronics, Winona Minnesota; David Pinsky, Amit Sarkhel, and Karen Ebner, Raytheon; Rob Tyrell, Stentech; Don Lockard, Yankee Soldering; Eric Ren and Deb Fragoza, EMC; Andy Lesko and Bernhard Wessling, Ormecon; Don Longworth, Tom Buck, Wendi Boger, and Brian Corbey, Dynamic Details Inc; Helena Pasquito and Dick Anderson, Cobham (M/A-COM); George Wilkish, Prime Consulting; Scott Miller, Wendy Milam, and Lauren Primmer, Freedom CAD; Crystal Wang, International Rectifier; Don Abbot, Texas Instruments; Ken Degan, Teradyne; Steven Sekanina, Isola; Mike Jansen, Mike Miller, Louis Feinstein, and Jim Daley, Textron Systems; Charlie Bickford, Wall Industries; Roger Benson, Carsem; and Tim O'Neill and Karl Seelig, Aim Solder. Also, we appreciate the efforts of Linda Darveau, U.S. EPA Region 1 for providing funding for this research.

References

[1] Pecht, Michael, Fukuda, Yuki, Rafagopal, Subramanian, The Impact of Lead-free Legislation Exemptions on the Electronics Industry, IEEE Transactions on Electronics Packaging Manufacturing, Vol. 27, No. 4, pp. 221 – 232, October 2004.

[2] European Union, Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment, Office Journal of the European Union, February 13, 2003.

[3] Shina Sammy G., “Six Sigma for Electronics Design and Manufacturing”, McGraw Hill, New York, May 2002.

[4] Shina, Sammy G., Green Electronics Design and Manufacturing – Reliability of Green Electronic Systems, McGraw-Hill, New York, 2008.

[5] Morose, Gregory, Sammy Shina, et al. “Visual and Reliability Testing Results of Circuit Boards Assembled with Lead Free Components, Soldering Materials and Processes in a Simulated Production Environment”, Submitted for APEX 2006 Conference.

[6] IPC Association Connecting Electronics Industries, IPC-9701: Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, January 2002.

Biographies

Gregory Morose has been managing the efforts of the New England Lead-free Electronics Consortium since 2004. Previously, Gregory had worked for several years in the electronics industry in various engineering positions. He has published and presented numerous papers about lead-free electronics research and implementation. He is also an ASQ certified Six Sigma Black Belt.

Sammy G. Shina, P.E., is a professor of Mechanical Engineering at the University of Massachusetts Lowell and the founder of the New England Lead Free Consortium. He is the author of four books on Concurrent Engineering, Six Sigma and Green Electronics Design and more than 100 papers on electronics assembly, quality, design, and manufacturing.

Robert Farrell is an Advanced Engineer who has been on the Benchmark Electronics Corporate Lead-free team since 2002 and has worked on-site at several Benchmark global locations as they converted from tin lead assembly to lead free. Bob has been an active member of the New England Lead Free Electronics Consortium since 2004. He has published and presented several lead free technical papers.